REMARKS

Claims 1-5 and 7-17 are pending in this application. Claims 11-17 are newly presented, and claims 1-5 and 7-10 have been rejected. Claims 5 and 10 have been amended to attend to matters of form. Claims 1, 8 and 11 are independent.

The Objection to the Claims

Claims 5 and 10 have been objected to on grounds certain features introduced therein already were recited in prior claims.

Claims 5 and 10 have been carefully reviewed and revised as appropriate to attend to the points noted by the Examiner. Accordingly, favorable reconsideration and withdrawal of this objection are respectfully requested.

The Rejections Under 35 U.S.C. § 103

Claims 1-5 and 8-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,610,635 to Murray et al. in view of U.S. Patent No. 5,838,549 to Nagata et al. Applicants respectfully traverse this rejection and submit the following arguments in support thereof.

As pointed out in the Amendment filed on April 25, 2005, Applicants' invention, as set out in claim 1, involves a circuit board having a storage device for storing data relating to a marking material for printing. The circuit board includes at least two ground terminals arranged at two edges of the circuit board that are located on one axis, and plural terminals arranged on the circuit board for read/write operations on the data relating to the marking material for printing. The terminals include a power supply terminal and a control signal terminal. At least two ground terminals are not the terminals in closest proximity to the power supply terminal.

It also has been previously noted that claim 8 describes a circuit board with a storage device for storing data relating to a marking material for printing, the board being provided to a marking material for a print cartridge having a substantially rectangular shape. The circuit board has two ground terminals arranged on the circuit board at two edges thereof along one side, and terminals arranged parallel to one side of the circuit board, and used for storing the data. The terminals include a power supply terminal and a control signal terminal. The ground terminals are not the terminals in closest proximity to the power supply terminal.

The Office Action **admits** that Murray does not disclose a configuration where at least two ground terminals are not the terminals in closest proximity to a power supply terminal; at page 3 the Office Action states "Murray et al. does not disclose wherein said at least two ground terminals are not the terminals in closest proximity to said power supply terminal".

The Office Action then attempts to remedy Murray's deficiency by applying Nagata, which is alleged to disclose a configuration where at least a ground terminal is not the terminal in closest proximity to a power supply terminal (Office Action, page 3, second full paragraph).

Nagata, however, provides no disclosure of **two** ground terminals as recited in present claim 1. As shown in Figs. 1 and 4, and as discussed at col. 6, lines 26-35, Nagata only teaches the use of an IC card in which one ground terminal Gnd is provided in association with the power terminal Vcc.

It is important to note that while the claimed invention provides for multiple ground terminals for each power supply terminal, Nagata only associates a **single** ground terminal with the power supply terminal (see Figs. 1, 4). Nowhere does Nagata suggest using two ground terminals, much less arranging the two ground terminals and the power supply terminal in the manner claimed. Consequently, Nagata does not even suggest the aspects of this

invention involving at least two ground terminals being arranged on the circuit board at two edges thereof located on one axis thereof, or the at least two ground terminals not being the terminals in closest proximity to the power supply terminal.

In fact, Nagata is not properly combined with Murray because Nagata only is concerned with and seeks to prevent the flow of short-circuit current through a memory module. Nagata describes this as follows in the Abstract:

> the power supply layer or grand [sic: ground] layer that is connected to either the power supply terminal Vcc or the ground terminal Gnd of each semiconductor memory, which is located farther from the connection terminals, is arranged closer to the semiconductor memories with this arrangement, the short circuit current flowing through the semiconductor memories is more strongly magnetically coupled with the power supply layer or ground layer arranged close to them. Thus, it is possible to reduce the effective inductance. This, in turn, reduces noise, making it possible to provide a semiconductor module with an increased processing speed.

It therefore is not appropriate to apply Nagata against the claimed invention, which is directed to contact with external terminals.

Still another reason why the claimed invention patentably distinguishes over the cited art is because, as the Examiner **admits**, Murray does not suggest the positional relation between ground terminals and a power supply terminal, and there is no motivation to combine Murray and Nagata.

Lastly, even if Murray is combined with Nagata, that combination still does not provide all the constituent features of claim 1, since neither of those references provides even a suggestion of the claimed positional relation between the two ground terminals and the power supply terminal.

For all the foregoing reasons, favorable reconsideration and withdrawal of this rejection are respectfully requested.

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Murray in view of Nagata as applied to claims 1 and 3-5, and further in view of U.S. Patent No. 5,748,179 to Ito et al. Applicants respectfully traverse this rejection and submit the following arguments in support thereof.

Claim 7 ultimately depends from, and so incorporates by reference all the features of claim 1, including those features shown above to avoid Murray and Nagata. Claim 7 therefore avoids Murray and Nagata at least for the reasons already given with regard to claim 1.

Ito only is cited as teaching a circuit board having plural terminals arranged at intervals of approximately 1 mm in the direction of formation of the rows.

Ito is directed to an LCD device having driving circuits with multilayer external terminals. As such, Ito is not properly combined with the other cited references. Moreover, the asserted justification for the combination of Ito with Murray and Nagata, "to reduce the noise interference due to the close position of the electrical terminals as well known in the art" is unsupported by Ito - nowhere in Ito is there even a suggestion that Ito's teachings reduce noise interference. Accordingly, if this rejection is to be maintained it is respectfully requested that the Examiner establish that Ito's teachings provide the benefit of noise reduction. Applicants respectfully submit that unless such a benefit can be shown, there is no basis to support the asserted combination of Ito with the other references.

Even assuming arguendo that Ito can be combined with Murray and Nagata, it remains that Ito does not remedy the above-noted deficiencies of those other references. Ito only relates to an LCD display - there is no suggestion that multiple ground terminals be provided, or that those ground terminals and the power supply terminal be arranged in the manner claimed.

Accordingly, the claimed invention avoids the combination of Murray, Nagata and Ito for the same reasons as already have been given with regard to claim 1.

For all the foregoing reasons, favorable reconsideration and withdrawal of this rejection are respectfully requested.

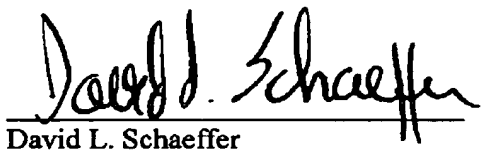
CONCLUSION

Applicants respectfully submit that all outstanding rejections have been addressed and are now either overcome or moot. Applicants further submit that all claims pending in this application are patentable over the prior art. Favorable reconsideration and withdrawal of those rejections and objections is respectfully requested.

No fees are believed to be due in connection with the filing of this Amendment. Nevertheless, should the Commissioner deem any fee(s) to be now or hereafter due, the Commissioner is authorized to charge all such fees due in this application to Deposit Account No. 19-4709.

In the event that there are any questions, or should additional information be required, please contact Applicant's attorney at the number listed below.

Respectfully submitted,



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